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(54) Bitline contacts in a memory cell array

(57) The present invention provides a method for providing bitline contacts in a memory cell array which comprises a plurality of bitlines (2) arranged in a first direction, said bitlines (2) being covered by an isolating layer (3), a plurality of wordlines (4) arranged in a second direction perpendicular to said first direction above said bitlines, memory cells being disposed at the points at which said bitlines (2) and wordlines (4) cross each other. The isolating layer (3) is removed from the bitlines (2) at the portions which are not covered by the wordlines (4), whereas the areas between the bitlines (2) remain unaffected in. An electrical conductive material (18) is provided on the exposed portions of said bitlines (2).

The method is used to provide bitline contacts in a nitride read only memory (NROM™) chip.

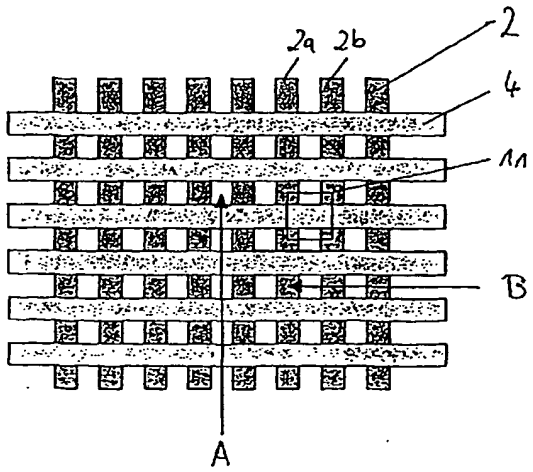

FIG.2

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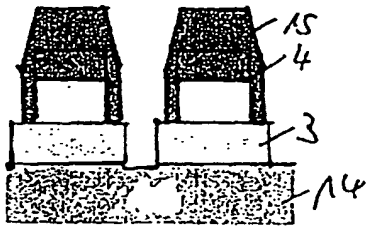

FIG. 7B

Description

[0001] The present invention relates to a method for providing bitline contacts in a memory cell array in which a plurality of bitlines is arranged in a first direction, said bitlines being covered by a silicon dioxide layer, a plurality of wordlines is arranged in a second direction perpendicular to said first direction above said bitlines, and memory cells are disposed at the points at which said bitlines and wordlines cross each other.

[0002] The present invention can very advantageously applied to NROM™ (nitride read only memory) cells which are for example known from US-A-5,966,603, US-A-5,768,192, US-A-6,133,095, and US-A-5,963,465.

[0003] Such an NROM™ cell is a charge trapping memory device, which can be seen as a simple sub-micron MOS transistor whose gate oxide is replaced with a thin oxide-nitride-oxide (ONO) multi-layer stack, as can be seen from Figure 1. In Figure 1, reference numeral 1 denotes a substrate, for example of p-doped silicon. N^+-doped bitlines 2 are arranged in a first direction, and they are covered by a thick silicon dioxide layer having a thickness of approximately 50 nm, also referred to as the bitline oxide 3. The word lines 4 made of polycide, a dual layer structure of tungsten silicide and polysilicon, are disposed in a second direction crossing the first direction. The second direction is preferably perpendicular to the first direction. The ONO multi-layer comprising a silicon dioxide layer 5, a silicon nitride layer 6, and a silicon dioxide layer 7, is disposed between the wordline 4 and the silicon substrate 1. A transistor having a channel 13 is formed between two adjacent bitlines 2 acting as source and drain electrode, the wordline 4 acting as the gate electrode and the ONO multi-layer acting as the gate isolator.

[0004] The intermediate layer of the ONO multi-layer stack, i.e. the nitride layer 6, is the retaining material for one or two distinguishable pockets of electrons, close to the bitline 2 junction edge.

[0005] For sake of simplicity the concept of the NROM™ cell is described for the storage of one electron only. However, currently, the NROM™ cell is also applied for the storage of two electrons.

[0006] Figure 2 shows a top view of a two-dimensional array of NROM™ cells, made of a crisscross of n^+-doped bitlines 2 and wordlines 4. The location of the trapped electron is near the bitline junction edge, as shown in Figure 1. Also shown is the memory cell 11 at the cross-section whose details are shown in Figure 1. The programming operation of the NROM™ cell is done by Channel Hot Electron injection, which stores a nominal less than a thousand electrons in a lumped pocket close to the drain side of the cell. These electrons are located in localized states in the nitride layer.

[0007] An electron 8, for example, is injected and trapped by applying a higher potential to the first bitline 2a than to the second bitline 2b, as is indicated by the programming direction 10. Additionally, a sufficient voltage is applied to the wordline 4. For reading the electron 8, a higher potential is applied to the second bitline 2b than to the first bitline 2a, as is indicated by the reading direction 9. Additionally, a low voltage is applied to the wordline 4.

[0008] As is obvious, the potential difference applied for reading is lower than the potential difference applied for programming. Since a comparatively high voltage is applied to the wordlines for programming, the thickness of the spacer which covers the wordlines must be thicker than in other known memory devices such as a DRAM (dynamic random access memory) in order to avoid a breakthrough between neighbouring wordlines or between a wordline and a bitline contact. In particular, typical voltages applied to the wordlines of NROM™ cells are approximately 12 Volts, whereas typical voltages applied to the wordlines of DRAM cells are 3 to 5 Volts.

[0009] Since the n^+-doped bitlines 2 exhibit a considerable resistance, according to a standard cell architecture, metal lines are disposed on top of the memory cell array in arrays having a certain magnitude. These metal lines are also arranged in the first direction above the bitlines 2, and they are periodically connected to the underlying bitline via a contact. For example, every 8th or 16th memory cell has a contact to the metal line so as to reduce the bitline resistance. Since these metal lines usually are very thick, they place a further restriction upon the shrinkage of the memory cell size.

[0010] Conventionally, the contact between bitline and metal line can be provided by a method in which after the formation of the wordlines the whole memory cell array is covered by a boron phosphorous silicate glass as well as a silicon dioxide layer. Then, the silicon dioxide layer, the boron phosphorous silicate glass as well as the underlying bitline oxide are etched at predetermined positions which are for example photolithographically defined using a mask having a hole pattern so as to provide the contact holes. Thereafter, the contact holes are etched selectively with respect to the wordlines, especially the nitride spacer and nitride cap of the gate electrodes. Accordingly, the lateral extension of the contact holes is essentially defined by the spacing between neighbouring wordlines. For this reason, this contact is called a self aligned contact (SAC).

[0011] This process involves two major disadvantages. On one hand, as explained above, the voltages applied to the wordlines of NROM™ cells are much higher than those applied to the wordlines of other known memory cells such as DRAM (dynamic random access memory) cells. Therefore, the nitride spacer and the cap nitride have to withstand much higher voltages and, thus, are made thicker. Consequently, the space between neighbouring wordlines is reduced and the aspect ratio of the contact holes is much increased. In more detail, since the silicon dioxide layer usually has a thickness of 500 nm, contact holes having a very high aspect ratio of 10 to 15 have to be etched. Thus, it becomes very difficult to entirely etch the silicon dioxide layer, the phosphorous boron silicate glass as well as the underlying

bitline oxide and, subsequently, fill the space between neighbouring wordlines.

[0012] On the other hand, the etching time has to be appropriately adjusted in order to avoid that the nitride spacer be etched too much. Accordingly, the process of etching the bitline oxide during the NROM™ fabrication is very critical. Unsufficient etching times will result in an unsufficient contact between bitline and bitline contact. However, for a better device performance, a low RC constant of the bitline contact is necessary in order to achieve a higher saturation current and a better signal detection. Moreover, excessive etching times will result in shorts between bitline contact and wordline which is a major problem in the fabrication of memory cell arrays.

[0013] By introducing a new etching gas, especially C_5F_8, having a higher selectivity of etching silicon dioxide deposited by the TEOS process with respect to silicon nitride, or by depositing a phosphorous boron silicon glass having a reduced thickness so that the stack which must be etched assumes a reduced height, the above problems can be partially solved. However, the results obtained still are not entirely satisfactory.

[0014] From T.H. Yoon et al., Symp. on VLSI Tech. Dig., 1999, p. 37, it is known to replace an SAC process by a so-called Pre Poly Plug process in which doped silicon is entirely deposited and patterned so as to provide a cell plug in a DRAM cell. However, as is obvious, a DRAM cell has a structure which is completely different from that of an NROM™ cell, and, in particular, there is no bitline oxide which has to be etched in order to provide a bitline contact.

[0015] It is an object of the present invention to provide an improved method for providing bitline contacts in a memory cell array such as an NROM™ chip. Moreover, it is an object of the present invention to provide an improved memory cell array as well as an improved NROM™ chip.

[0016] According to the present invention, the above object is achieved by a method for providing bitline contacts in a memory cell array comprising a plurality of bitlines arranged in a first direction, said bitlines being covered by an isolating layer, a plurality of wordlines arranged in a second direction crossing said first direction above said bitlines, memory cells being disposed where said bitlines and wordlines cross each other, said method comprising the steps of removing said isolating layer from the bitlines at the portions which are not covered by the wordlines, whereas the areas between the bitlines remain unaffected, and providing an electrical conductive material on the exposed portions of said bitlines.

[0017] In addition, the present invention provides a method for providing bitline contacts in a nitride read only memory (NROM™) chip, said memory chip comprising a memory cell array in which a plurality of memory cells are disposed at the points at which a plurality of bitlines, which are covered by an isolating layer, arranged in a first direction and a plurality of wordlines arranged in a second direction perpendicular to said first direction cross each other, each of said memory cells being composed of an metal-insulator-semiconductor field effect transistor wherein said insulator is an oxide-nitride-oxide multi-layer stack for storing one or more injected electrons, and a peripheral portion comprising logic components, said method comprising the steps as defined above.

[0018] Moreover, the present invention provides a memory cell array as well as a nitride read only memory (NROM™) chip having bitline contacts produced by the method as defined above, respectively.

[0019] More specifically, according to the present invention, the isolating layer is completely removed from the bitlines at the portions which are not covered by the wordlines whereas the areas between the bitlines remain unaffected. This is in contrast to the known methods in which the isolating layer is only partially removed at those portions which are photolithographically defined by a hole mask.

[0020] Therefore, according to a preferred embodiment of the present invention, a mask having a stripe pattern and, in particular, the bitline mask for defining the bitlines, can be used for patterning the photoresist material coated onto the memory cell array. However, the alignment of a mask having a stripe pattern is much easier than the alignment of a mask having a hole pattern. As a consequence, the present invention provides a method by which a misalignment is avoided and the bitline oxide is exactly removed from the bitlines.

[0021] Moreover, according to a preferred embodiment of the present invention, the electrical conductive material is provided on the exposed portions of the bitlines by an inverse poly etching process, in which, first, doped polysilicon is deposited over the whole cell array and, then, the doped polysilicon is removed from the areas between the bitlines. To this end, the doped polysilicon is advantageously covered by a photoresist material which is then patterned using a mask having a stripe pattern.

[0022] This inverse poly etching process is particularly advantageous since in contrast to known methods, in which contact holes are etched into an isolating material, the polysilicon is only removed at the areas between the bitlines. Therefore, according to this embodiment of the present invention, a self aligned contact etch is not performed, and the spacer and cap nitride on the gate electrodes are not attacked whereby shorts between bitlines and wordlines are avoided. In addition, the aspect ratio of the bitline contacts can be increased. As a consequence, the thickness of the spacers on the wordlines can be increased.

[0023] Again, since a mask having a stripe pattern is used, a misalignment of the mask can be largely avoided. Accordingly, an overlay mistake does not occur.

[0024] In particular, when the present invention is applied to a nitride read only memory cell array, the increased thickness of the spacer is highly advantagous since the gate electrodes in these cell arrays have to withstand much

higher voltages than, for example, in DRAM cell arrays.

[0025] The memory cell array as well as the nitride read only memory cell array of the present invention are different from the known memory cell arrays and nitride read only memory cell arrays, respectively, since the bitlines are electrically connected with overlying metal lines via conducting bitlines at each of the memory cells. Due to the special manufacturing method comprising the inverse poly etching process of the present invention, the bitline contacts are not formed at every 3rd or 4th memory cell as is the case when the conventional SAC process using a contact hole mask is applied, but the bitline contacts are formed at every memory cell.

[0026] The memory cell array as well as the nitride read only memory cell array of the present invention are especially advantageous with respect to the known ones since they exhibit an improved resistance to shorts between wordlines and bitlines due to their increased spacer thickness.

[0027] The method for providing bitline contacts in a memory cell array can be applied to any cell type in which the bitline is covered by an isolating layer such as a bitline oxide. Typical cell types to which the present invention can be applied include ROM and EPROM cells.

[0028] In the following, the present invention will be described in more detail with reference to the accompanying drawings.

Figure 1	shows a cross-sectional view of an NROM™ memory cell;
Figure 2	shows an exemplary memory cell array to which the present invention can be applied;
Figures 3 and 4A to 4C	illustrate the steps for preparing an NROM™ memory cell array according to known methods;
Figures 5 to 7	illustrate the steps of removing the bitline oxid in the method for providing a bitline contact according to the present invention; and
Figures 8 to 10	illustrate the steps of providing an electrical conductive material in the method for providing a bitline contact according to the present invention.

[0029] The following description of the preferred embodiment of the present invention will mainly focus on the process of manufacturing an NROM™ memory cell array, in which essentially the steps of creating the memory cell components are described whereas the definition of the peripheral parts of the memory cell array comprising logic components is only schematically outlined. As is clearly to be understood, the peripheral parts of the memory cell array are manufactured by generally known methods.

[0030] An ONO multi-layer comprising a 5 nm to 15 nm SiO_2 layer 5, a 2 to 15 nm Si_3N_4 layer 6 and a 5 to 15 nm SiO_2 layer 7 is deposited by conventional processes on a semiconductor substrate 1, for example of p-doped silicon, so that the entire substrate is covered with an ONO multi-layer as is shown in Figure 3.

[0031] Thereafter, a bitline mask which is typically photoresist patterned in a well known manner is deposited on the substrate in order to create the bitlines, forming lines of source electrodes and lines of drain electrodes. The layout of the bitline mask within the memory cell array portion of the chip is shown in Figure 4A. As is shown in Figure 4B, the photoresist columns 12 define the areas where the bitlines 2 are not to be implanted. Accordingly, they are disposed at the channel regions 13 of the transistors as is shown in Figure 1.
Figure 4C shows a cross section of the memory cell having the implanted bitlines.

[0032] Next, the top oxide 7 and the nitride layer 6 are etched from the regions between the photoresist columns 12, typically by a dry etching process. Thereafter, the bitlines 2 are implanted in the areas between the photoresist columns 12 with an n-dopant. By this process, the bitlines 2 are implanted in a self-aligned manner with respect to the photoresist columns 12.

[0033] Then, the photoresist columns 12 are removed, the ONO multi-layer is removed from the peripheral parts of the chip and a thermal oxidation process is performed. Thereby, bitline oxides 3 are thermally grown over the bitlines 2. Since the growth rate is much higher on the highly doped bitlines than on the nitride and oxide layers 6, 7, a thick layer of silicon dioxide is grown over the bitlines whereas a thin layer of silicon dioxide is grown along the sides of the nitride layer 6 and a thin layer of silicon dioxide is grown over the oxide layer 7. Moreover, a silicon dioxide layer acting as a gate isolating layer is grown in the peripheral portion of the chip.

[0034] A bitline oxide thickness of 20 to 70 nm is considered appropriate. Figure 4C shows a cross sectional view of the resulting structure.

[0035] Then, a polysilicon layer which will create wordlines of the memory cell array portion and will create gates for the peripheral transistors, is laid down over the chip. In the next step, a low resistive silicide, for example tungsten silicide, is deposited over the polysilicon layer so as to form a polycide layer having a reduced resistance. A typical total thickness of the polycide layer amounts to 100 to 200 nm. As shown in Figure 2 the polycide layer is then etched using a mask. Thereby, wordlines 4 are defined within the memory cell array, whereas gate electrodes are defined in the peripheral portion.

[0036] The resultant memory cell structure is shown in Figure 1.

The polycide layer 4 lies on top of the ONO multi-layers, thereby forming the gates of the NROM™ cells. The bitline oxides 3 are thick enough to isolate neighbouring ONO multi-layers.

[0037] Thereafter, a side wall oxidation step for the wordlines 4, a lightly doped drain (LDD) implant procedure into the CMOS periphery only and a spacer 15 deposition are performed. The LDD typically requires separate masks for the n-channel and p-channel peripheral transistors.

[0038] In NROM™ cells, the nitride spacer on the gate electrode should be thicker than the nitride spacer thickness of DRAM or embedded DRAM cells since they have to withstand a higher voltage due to the higher voltage applied to the gate electrodes. It is estimated that the spacer thickness should exceed 40 nm.

[0039] After forming this spacer, a nitride liner as well as a thick silicon dioxide spacer are deposited over the whole chip area. The thick silicon dioxide spacer which is formed by a chemical vapour deposition process using tetraethyl-orthosilicate (TEOS) is used for the transistors built in the peripheral portion. Thereafter, the thick silicon dioxide spacer is removed from the memory cell portion of the chip.

[0040] In the next step, the process of the present invention will be performed so as to define the bitline contacts for contacting the bitlines with metal lines which are to be formed later.

[0041] Figure 5A shows a cross sectional view of the memory cell array along direction A as defined in Figure 2, whereas Figure 5B shows a cross sectional view of the memory cell array along direction B as defined in Figure 2. Reference numeral 14 denotes the active areas of the memory cell array. Figure 5C shows a cross sectional view of the logic devices arranged in the peripheral part of the chip.

[0042] The nitride liner which was deposited after forming the nitride spacer may be completely or partially removed at those locations at which the bitline oxide is to be etched.

[0043] First, a thin silicon dioxide layer 16 having a thickness of approximately 10 to 25 nm is deposited over the whole chip (Figure 6B). As an alternative, if the nitride liner has only partially been removed, the step of depositing a thin silicon dioxide layer can also be omitted.

[0044] Then, a photoresist material 17 (Figure 6C) is coated onto the whole chip and it is patterned using the bitline implantation mask as shown in Figure 4A. As a result, the photoresist is removed in those portions at which originally the bitlines 2 were defined, whereas in the remaining areas between the bitlines 2 the photoresist material remains. As can be seen from Figure 6A which shows a cross sectional view of the resultant memory cell array along direction A as defined in Figure 2, the portions at which the photoresist material is removed have a more narrow width than the bitlines 2 which is due to the impurity diffusion during the thermal steps performed before. Accordingly, the misalignment which occurs when laying the bitline mask over the photoresist layer is smaller than the broadenening of the bitlines due to impurity diffusion. As a consequence, the portions at which the photoresist material is removed lie exactly above the bitlines and not between them so as to make sure that exactly the bitline oxide will be removed in the next steps.

[0045] As can be seen from Figure 6B which shows a cross sectional view of the resultant memory cell array along direction B as defined in Figure 2, the photoresist material is completely removed from the wordlines 4 in the bitline areas. As shown in Figure 6C which shows a cross sectional view of the logic devices arranged in the peripheral portion of the chip, the peripheral portion is completely protected by the photoresist material.

[0046] In the next step, the silicon dioxide is selectively etched with respect to silicon. In order to avoid that the nitride spacer of the gate electrodes will be attacked, it is important that the silicon dioxide is etched selectively with respect to silicon nitride. Since the silicon dioxide is selectively etched with respect to silicon the implanted bitlines will not be substantially attacked by this etching process. Thereafter, the photoresist material is completely removed.

[0047] As a result, the silicon dioxide is removed in those portions at which originally the bitlines 2 were defined, whereas the areas between the bitlines 2 remain unaffected. As can be seen from Figure 7A which shows a cross sectional view of the resultant memory cell array along direction A as defined in Figure 2, at the portions at which the photoresist material has been removed in Figure 6A, the silicon dioxide now is removed thus creating the contact holes for the bitline contacts.

[0048] As shown in Figure 7B which shows a cross sectional view of the resultant memory cell array along direction B as defined in Figure 2, the bitline oxide 3 between adjacent wordlines now is completely removed in the bitline areas. Since the bitline oxide was etched selectively with respect to silicon nitride and, in addition, the wordlines were covered by an isolating layer such as made of silicon dioxide before depositing the photoresist material, the spacer on the wordlines is not attacked by this etching step.

[0049] As shown in Figure 7C which shows a cross sectional view of the logic devices arranged in the peripheral part of the chip, the silicon dioxide layer remains over the wordlines in this area.

[0050] As a further modification of the described process steps, the spacer of the gate electrodes may as well be formed of silicon dioxide if the silicon nitride liner which is deposited thereafter is not removed from these areas. Accordingly, the silicon nitride liner protects the underlying silicon dioxide spacer from etching. Since silicon dioxide has a higher resistance to breakthrough, the use of a silicon dioxide spacer is highly advantageous.

[0051] In the next steps, an electrical conductive material will be provided on the exposed portions of the bitlines. This can be done by a conventional process, which provides self aligned contacts as was outlined above, or, according

to a preferred embodiment of the present invention, by a so-called inverse poly etch as will be explained later.

[0052] For providing the electrical conductive material in the contact hole by a conventional process, first, a silicon oxynitride liner followed by a boron phosphorous silicate glass (BPSG) is deposited over the entire chip area. Thereafter, a silicon dioxide layer is deposited by a chemical vapour deposition process using TEOS (tetraethylorthosilicate). In this layer stack, the contact holes will be etched.

[0053] Then, a photoresist material is coated and the contact holes for contacting the bitlines are lithographically defined using a contact hole mask. The contact hole mask is designed so that every 3rd or 4th memory cell is connected with the metal lines which are to be formed later. After defining the contact holes in the photoresist layer, the silicon dioxide layer as well as the BPSG material are selectively etched, for example by dry etching with C_4F_8 or C_5F_8.

[0054] In a following step, the photoresist material is removed from the cell area and, optionally, an ion implantation step with arsenic ions is performed so as to reduce the contact resistance.

[0055] In the next step, an electrical conductive material such as n^+-doped polysilicon is deposited so as to fill the contact holes. Then, the polysilicon on the chip surface is recessed, for example by wet etching or plasma etching using the BPSG layer as an etch stop layer. Thereafter, the metal lines will be formed in a manner that will be described later.

[0056] According to a preferred embodiment of the present invention, the electrical conductive material can also be filled into the contact holes by a so-called inverse poly etch process in which a doped polysilicon layer is deposited over the whole chip area, and this polysilicon layer is removed from those portions at which no contact is to be made.

[0057] First, a wet cleaning process is performed in order to remove silicon dioxide residues as well as a native oxide from the silicon surface, so that the doped polysilicon layer will be directly deposited on the silicon surface. Thereafter, a highly n-doped polysilicon layer 18 is deposited so as to cover the whole chip area. Next, a chemical mechanical polishing step with a target of approximately 100 nm above the nitride cap of the wordline is performed. The resulting structure is shown in Figures 8A to 8C, wherein Figure 8A shows a cross sectional view of the memory cell array along direction A as defined in Figure 2, Figure 8B shows a cross sectional view of the memory cell array along direction B as defined in Figure 2, and Figure 8C shows a cross sectional view of the logic devices arranged in the peripheral portion of the chip.

[0058] Thereafter, a hardmask layer 19 of silicon nitride having a thickness of approximately 200 nm is deposited, and a photoresist material (not shown) is coated. Using a mask having a stripe pattern, for example a mask similar to that shown in Figure 4a, the photoresist material is patterned so that in the resulting photoresist pattern the areas between the bitlines 2 are exposed. The mask having a stripe pattern can for example be generated using the bitline mask. Then, in the exposed areas between the bitlines 2, the hardmask layer 19 is removed and the n^+-doped polysilicon 18 is removed by etching. In a following step, the photoresist material will be removed.

[0059] After removing the photoresist material, a structure as shown in Figures 9A to 9C is obtained, wherein Figure 9A shows a cross sectional view of the memory cell array along direction A as defined in Figure 2, Figure 9B shows a cross sectional view of the memory cell array along direction B as defined in Figure 2, and Figure 9C shows a cross sectional view of the logic devices arranged in the peripheral part of the chip. As can be clearly seen from Figures 9A and 9B, the polysilicon 18 remains only at those portions above the bitlines 2, whereas it is completely removed over the logic components in Figure 9C. Since a thin silicon dioxide layer 16 was deposited before removing the bitline oxide, the peripheral portion is protected from etching.

[0060] Thereafter, a boron phosphorous doped silicate glass (BPSG) layer 20 is deposited over the entire chip area and it is planarized using chemical mechanical polishing using the silicon nitride hardmask as a polish stop. The resultant structure is shown in Figures 10A to 10C, wherein Figure 10A shows a cross sectional view of the memory cell array along direction A as defined in Figure 2, Figure 10B shows a cross sectional view of the memory cell array along direction B as defined in Figure 2, and Figure 10C shows a cross sectional view of the logic devices arranged in the peripheral part of the chip.

[0061] Accordingly, the bitline contacts are completed by providing an electrical conductive material by a method in which, first, the material is deposited over the whole chip area and, then, it is removed from the areas at which a contact is not to be made. As a consequence, a self aligned etching step in which the wordlines act as an etching mask and, thus, could be attacked, does not occur. Since the etching step is not self aligned, the width between the word lines can be further reduced so that the thickness of the spacers on the gate electrodes can be increased. As a consequence, shorts between wordlines and bitline contacts can be largely avoided whereby the device performance is greatly improved.

[0062] After removing the silicon nitride hardmask, the metal lines will be formed. The metal lines can be formed using the so-called damascene technique or any other arbitrary process. For creating the metal lines using the so-called damascene technique, first a silicon dioxide layer is deposited onto the entire chip area by a chemical vapour deposition process using tetraethylorthosilicate. Thereafter, trenches are etched into the silicon dioxide layer using a mask having a stripe pattern, for example the mask as used for defining the bitline contacts or a similar mask.

[0063] Then, a titanium liner and a layer of tungsten are deposited and the trenches are filled with these metals.

Finally, the surface is planarized using chemical mechanical polishing or etching back of the metal so that the trenches are completely filled and no metal remains in the spaces between the trenches so that the trenches are electrically isolated from each other.

[0064] According to a different process, it is also possible to first deposite a titanium liner and the tungsten material, deposit a photoresist material, lithographically define the metal lines using a mask having a stripe pattern, for example the bitline mask, etch the metal layers and deposit silicon dioxide in order to electrically isolate the metal lines from each other.

[0065] Thereafter, the memory chip is completed in a conventional manner.

Claims

1. A method for providing bitline contacts in a memory cell array comprising a plurality of bitlines (2) arranged in a first direction, said bitlines (2) being covered by an isolating layer (3), a plurality of wordlines (4) arranged in a second direction crossing said first direction above said bitlines (2), memory cells being disposed where said bitlines and wordlines cross each other,
   said method comprising the steps of:

   - removing said isolating layer (3) from the bitlines (2) at the portions which are not covered by the wordlines (4), whereas the areas between the bitlines (2) remain unaffected; and
   - providing an electrical conductive material (18) on the exposed portions of said bitlines.

2. The method for providing bitline contacts in a memory cell array according to claim 1, wherein the step of removing the isolating layer (3) from the bitlines (2) comprises the steps of:

   - depositing a photoresist material (17),
   - patterning said photoresist material (17) using a mask having a stripe pattern, and
   - selectively etching the isolating layer (3) with respect to the wordlines (4).

3. The method for providing bitline contacts in a memory cell array according to claim 2, wherein said mask having a stripe pattern is the bitline mask by which the bitlines (2) have been defined before.

4. The method for providing bitline contacts in a memory cell array according to any of claims 1 to 3, wherein the step of providing an electrical conductive material (18) on the exposed portions of said bitlines comprises the steps of:

   - depositing an isolating material onto the memory cell array;
   - coating a photoresist material and lithographically defining the contact holes in said photoresist material;
   - etching said isolating material so as to create said contact holes; and
   - depositing an electrical conductive material so as to fill said contact holes with said electrical conductive material.

5. The method for providing bitline contacts in a memory cell array according to any of claims 1 to 3, wherein the step of providing an electrical conductive material (18) on the exposed portions of said bitlines comprises the steps of:

   - depositing said electrical conductive material (18) onto the memory cell array;
   - removing said electrical conductive material (18) from the areas between the bitlines; and
   - depositing an isolating material (20) in the areas between the bitlines.

6. The method for providing bitline contacts in a memory cell array according to claim 5, wherein the step of removing said electrical conductive material (18) from the areas between the bitlines (2) comprises the steps of:

   - coating a photoresist material on said electrical conductive material and lithographically defining the regions where the electrical conductive material is to be removed using a mask having a stripe pattern; and
   - removing the electrical conductive material (18) in the exposed regions.

7. The method for providing bitline contacts in a memory cell array according to any of claims 2 to 6, wherein said

isolating material (20) is a silicate glass doped with boron and/or phosphorous.

8. The method for providing bitline contacts in a memory cell array according to any of claims 1 to 7, wherein said electrical conductive material (18) is doped polysilicon.

9. A method for providing bitline contacts in a nitride read only memory (NROM) chip, said memory chip comprising

- a memory cell array in which a plurality of memory cells are disposed at the points at which a plurality of bitlines (2), which are covered by an isolating layer (3), arranged in a first direction and a plurality of wordlines (4) arranged in a second direction perpendicular to said first direction cross each other, each of said memory cells being composed of an metal-insulator-semiconductor field effect transistor wherein said insulator is an oxide-nitride-oxide multi-layer stack for storing one or more injected electrons, and
- a peripheral portion comprising logic components, said method comprising the steps as defined in any of claims 1 to 8.

10. A memory cell array having bitline contacts produced by the method of any of claims 1 to 8.

11. A nitride read only memory (NROM) chip having bitline contacts produced by the method of claim 10.

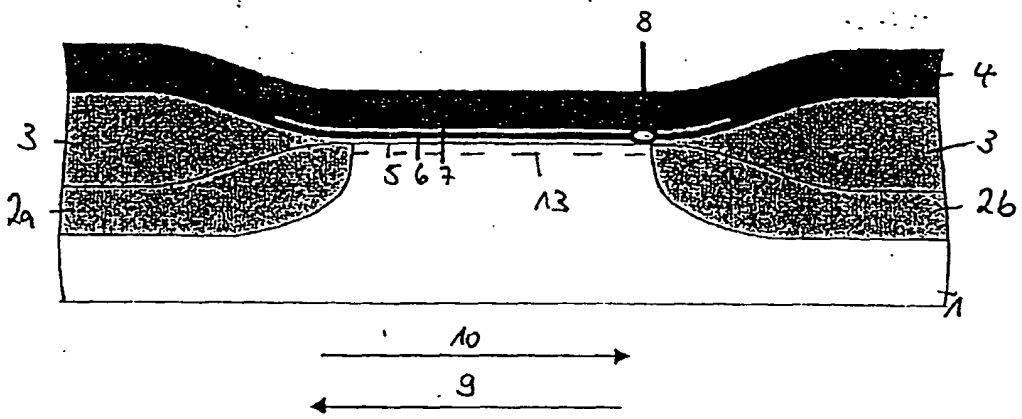

FIG. 1

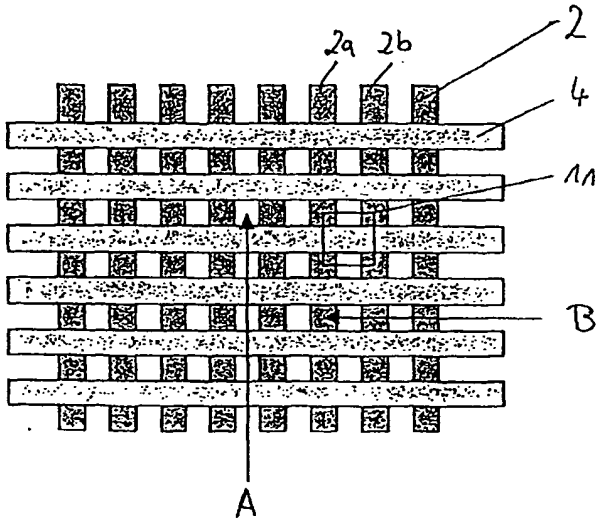

FIG. 2

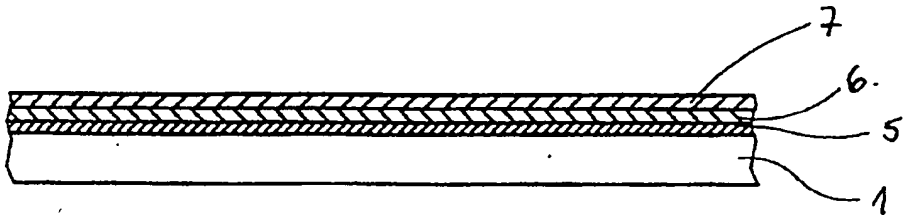

FIG.3

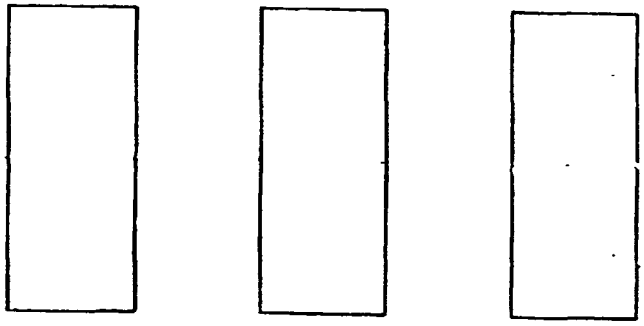

FIG. 4A

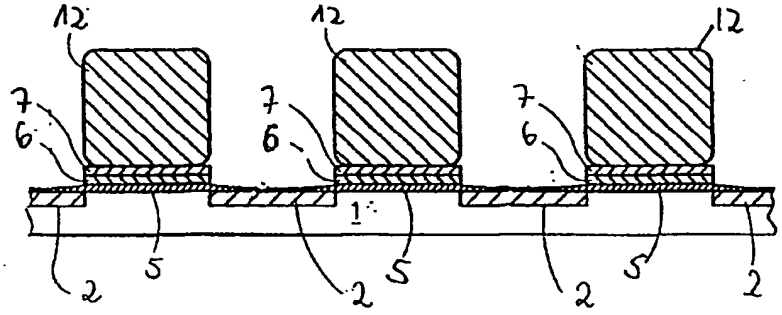

FIG. 4B

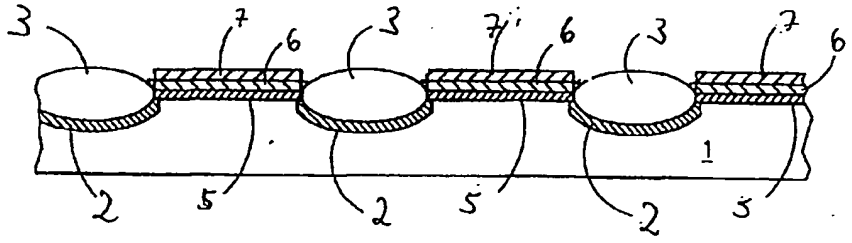

FIG. 4C

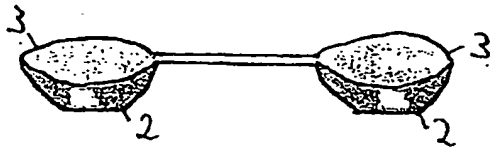

FIG. 5A

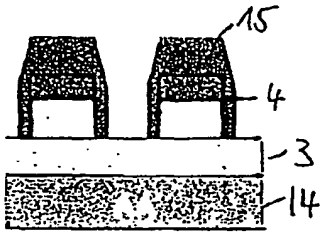

FIG. 5B

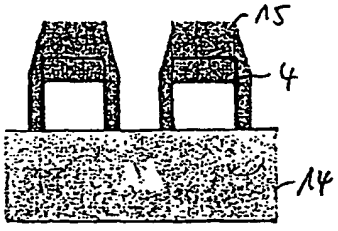

FIG. 5C

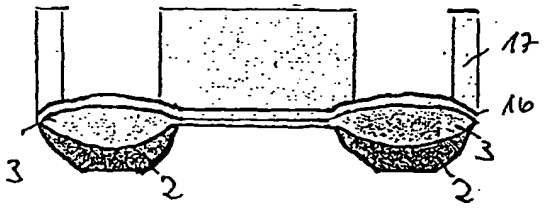

FIG.6A

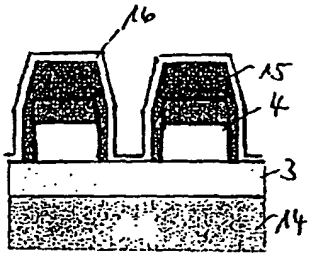

FIG.6B

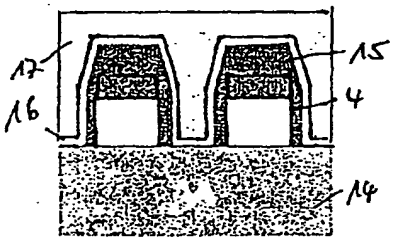

FIG.6C

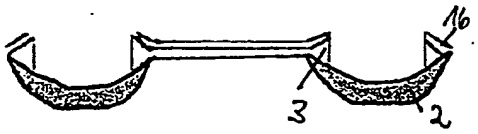

FIG. 7A

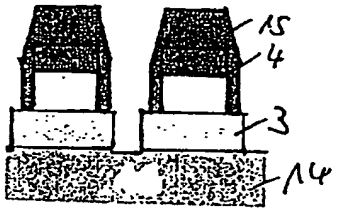

FIG. 7B

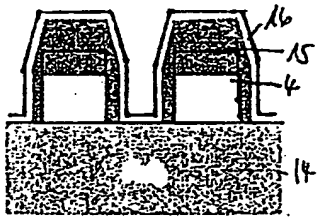

FIG. 7C

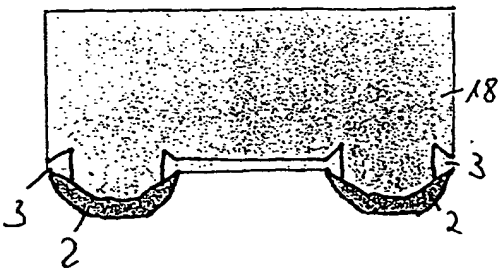

FIG.8A

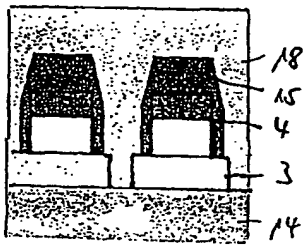

FIG.8B

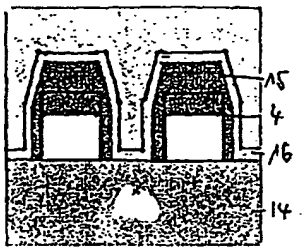

FIG.8C

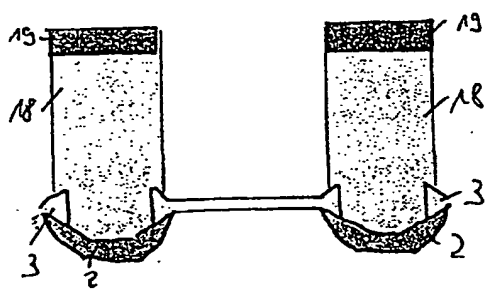

FIG.9 A

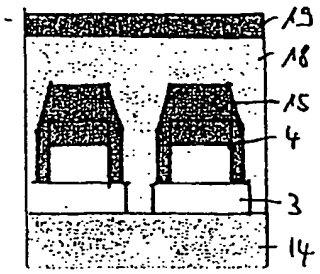

FIG.9B

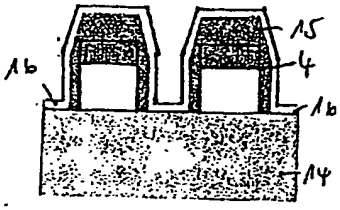

FIG.9C

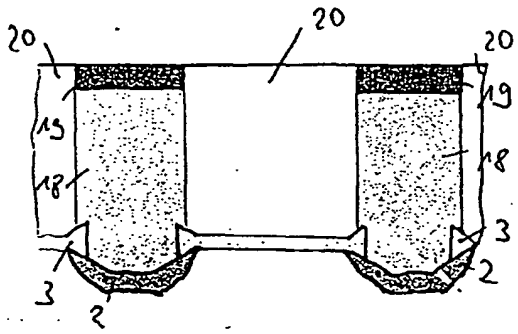

FIG. 10 A

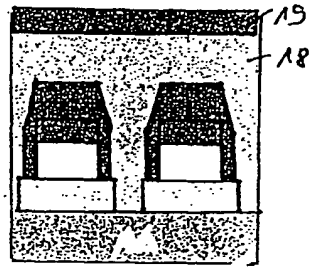

FIG. 10 B

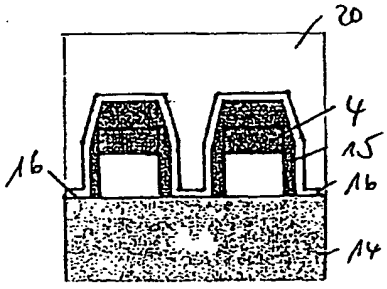

FIG. 10C

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 11 3179

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	US 5 168 334 A (MITCHELL ALLAN T ET AL) 1 December 1992 (1992-12-01) * the whole document *	1-4,7-11	H01L27/105 H01L21/8239
A		5,6	H01L27/112 H01L21/8246
Y	US 5 915 203 A (BOTHRA SUBHAS ET AL) 22 June 1999 (1999-06-22) * the whole document *	1-4,7-11	H01L21/768
A	US 5 815 433 A (TAKEUCHI NOBUYOSHI) 29 September 1998 (1998-09-29) * the whole document *	1-11	
D,A	US 5 966 603 A (EITAN BOAZ) 12 October 1999 (1999-10-12) * abstract *	1,8-11	
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TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 November 2001	Albrecht, C

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